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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/910,531	07/20/2001	Steven C. Miller	062986.0212	2116

7590 03/09/2005

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EXAMINER	
BAKER, PAUL A	

ART UNIT	PAPER NUMBER
2188	

DATE MAILED: 03/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/910,531	MILLER ET AL.	
	Examiner	Art Unit	
	Paul A Baker	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 November 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☐ Claim(s) _____ is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *01/13/2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

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DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 18-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Barroso et al, US PGPUB 2004/0088487.

In regards to claim 18, Barroso discloses an input/output (I/O) interface, comprising:

a peripheral communications port in figure 2 element 250;

a local cache operable to store copies of data from a processor memory coupled to the I/O interface in figure 2 element 211; and

a resource manager operable to invalidate outdated data from the local cache maintain coherence with the processor memory in paragraph 51.

In regards to claim 19, Barroso discloses the interface is a Peripheral Component Interconnect (PCI) interface in figure 2 element 250.

In regards to claim 20, Barroso discloses the resource manager further operable to invalidate copies of data from the local cache in response to instructions from the processor memory in paragraph 51.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-4, 6-7, 9-13, 15-16, 21-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Barroso et al, US PGPUB 2004/0088487 in view of Bourne et al. US PGPUB 2003/0120875.

In regards to claim 1, Barroso discloses a multiprocessor system, comprising:

a processing sub-system including a plurality of processors and a processor memory system in figure 1 elements 110, 132;

a scalable network operable to couple the processing sub-system to an input/output (I/O) sub-system in figure 3 element 10 interconnection to element 20;

the I/O sub-system including a plurality of I/O interfaces in figure 3 element 20 peripheral connections;

the I/O interfaces each operable to couple a peripheral device to the multiprocessor system and to store copies of data from the processor memory system in the local cache for use by the peripheral device figure 2, I/O BUS and element 211; and

a coherence domain comprising the processors and processor memory system of the processing sub-system and the local caches of the I/O sub-system in paragraph 12.

Barroso does not disclose the local caches of the I/O subsystem operable to participate in the coherence domain through timed access to data in the processor memory system. Bourne discloses timed access to data elements in a multiprocessor system in figures 3 and 16 and paragraphs 120-127, these cache systems are part of a front end web application server (figure 2 element 202) which serve requests for data composed of data stored in back end servers (figure 2 element 212). Bourne discloses that data, which is dynamic in nature, benefits from time stamping data as a means for maintaining coherence with changing data. Therefore, it would have been obvious to one of ordinary skill in the art to incorporate Bourne's timed access of data for an I/O processor for the purpose of maintaining coherence of the data.

In regards to claim 2, Barroso discloses at least one of the I/O interfaces comprises a Peripheral Component Interconnect (PCI) interface in figure 2 element 250.

In regards to claim 3, Barroso discloses the scalable network comprises a plurality of routers in figure 2 element 243 and figure 1 element 143.

In regards to claim 4, Barroso discloses the processor memory system comprising a plurality of discrete processor memories in figure 1 element 132.

In regards to claim 6, Barroso discloses the processor memory system including a directory operable to identify data cached in an I/O interface in paragraph 51.

In regards to claim 7, Barroso discloses the processor memory system operable to invalidate copy of data stored in a local cache of an I/O interface response to a request for the data by a processor in paragraph 64, a request for exclusive access to data located within an I/O cache requires invalidation of that data as required by the MESI cache coherency protocol disclosed in Barroso in paragraph 42.

In regards to claim 9, Barroso discloses a method for maintaining data at input/output (I/O) interfaces of a multiprocessor system, comprising:

coupling a plurality of processors to a processor memory system in figure 1 element 110 connected to element 132 via element 122;

coupling a plurality interfaces to the processor memory in figure 3 element 20;

coupling a peripheral device to each interface in figure 3 disks attached to element 20;

caching copies of data in the processor memory system in the I/O interfaces for use by the peripheral devices in figure 2 element 211; and

maintaining coherence between the copy of data in the I/O interfaces and data the processor memory system in paragraph 12.

Barroso does not disclose the local caches of the I/O subsystem operable to participate in the coherence domain through timed access to data in the processor memory system. Bourne discloses timed access to data elements in a multiprocessor system in figures 3 and 16 and paragraphs 120-127, these cache systems are part of a front end web application server (figure 2 element 202) which serve requests for data composed of data stored in back end servers (figure 2 element 212). Bourne discloses that data, which is dynamic in nature, benefits from time stamping data as a means for maintaining coherence with changing data. Therefore, it would have been obvious to one of ordinary skill in the art to incorporate Bourne's timed access of data for an I/O processor for the purpose of maintaining coherence of the data.

In regards to claim 10, Barroso discloses at least one of the interfaces comprises a Peripheral Component Interconnect (PCI) interface in figure 2 element 250.

In regards to claim 11, Barroso discloses coupling the I/O interfaces to the processor memory system through a scalable network in figure 3 element 10 interconnection to element 20.

In regards to claim 12, Barroso discloses coupling the I/O interfaces the processor memory system through a scalable network comprising a plurality of routers in figure 2 element 243 and figure 1 element 143.

In regards to claim 13, Barroso discloses the processor memory system comprises a plurality of discrete processor memories in figure 1 element 132.

In regards to claim 15, Barroso discloses identifying in the processor memory system data having a copy cached in the I/O interfaces in paragraph 51.

In regards to claim 16, Barroso discloses invalidating a copy of data cached an I/O interface in response to a request by a processor for the data; and

releasing the data to the processor after invalidation of the copy in the I/O interface in paragraph 64, a request for exclusive access to data located within an I/O cache requires invalidation of that data as required by the MESI cache coherency protocol disclosed in Barroso in paragraph 42.

In regards to claim 21, Bourne et al. discloses invalidating cache entries in an I/O cache when an associated time period of the cache entry expires in figure 16.

In regards to claim 22, Barroso discloses a method for interfacing a peripheral device with a multiprocessor system, comprising:

storing copies of data in a processor memory system of the multiprocessor system in a local I/O memory at an interface for the peripheral device in figure 2 element 211; and

maintaining coherence between data in the processor memory system and copies of data in the local I/O memory in paragraph 12.

Barroso does not disclose the local caches of the I/O subsystem operable to participate in the coherence domain through timed access to data in the processor memory system. Bourne discloses timed access to data elements in a multiprocessor system in figures 3 and 16 and paragraphs 120-127, these cache systems are part of a front end web application server (figure 2 element 202) which serve requests for data composed of data stored in back end servers (figure 2 element 212). Bourne discloses that data, which is dynamic in nature, benefits from time stamping data as a means for maintaining coherence with changing data. Therefore, it would have been obvious to one of ordinary skill in the art to incorporate Bourne's timed access of data for an I/O processor for the purpose of maintaining coherence of the data.

In regards to claim 23, Bourne et al. discloses invalidating cache entries in an I/O cache when an associated time period of the cache entry expires in figure 16.

In regards to claim 24, Barroso discloses further comprising maintaining coherence between data in the processor memory system and copies of data in the

local I/O memory by at least removing copies data from the local I/O memory in response to instructions from the processor memory system in paragraph 51.

In regards to claim 25, Bourne et al. discloses invalidating cache entries in an I/O cache when an associated time period of the cache entry expires in figure 16.

Claims 5 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Barroso et al, US PGPUB 2004/0088487 in view of Bourne et al. US PGPUB 2003/0120875 in further view of Culler et al. "Parallel Computer Architecture".

In regards to claims 5 and 14, Barroso does not disclose the discrete processor memories are each dedicated to a processor. Barroso discloses a variant of the Non-Uniform Memory Architecture (NUMA), wherein memory access time between an intra-node memory access time is not equal an inter-node memory access. However all intra-node memory accesses are equal (UMA or SMP). Culler discloses in figure 8.4 the different variations of NUMA systems (Barroso's architecture is 8.4b). Figure 8.4c shows a NUMA configuration in which each processor has it's own dedicated memory. The benefits and drawbacks of snooping vs. directory based cache coherency schemes are well known in the art (primarily that snooping requires less die space (and all associated benefits such as reduced cost, lower power consumption, etc.) but does not scale very well beyond a certain number of nodes since snooping injects more traffic on the interconnects compared with directory based approaches). For Barroso's system,

the eight processors are approximately the maximum number of nodes a snooping interconnect can have before scalability becomes an issue. If one of ordinary skill in the art were to scale Barroso's node depicted in figure 1 to 16 or more processors (assuming 2^n processors per node), it would be obvious to them (at the time of applicant's invention) to migrate Barroso's Snooping-Directory based NUMA system to a Directory-Directory NUMA system. This migration does not affect the operation of any portion of Barroso's invention that has been used to reject applicant's claimed invention. Therefore it would have been obvious to one of ordinary skill in the art at the time of invention to have each processor posses it's own discrete memory.

Claims 8 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Barroso et al, US PGPUB 2004/0088487 in view of Bourne et al. US PGPUB 2003/0120875 in further view of Sharma et al. US Patent 6,085,263.

In regards to claim 8, Barroso does not disclose the I/O interfaces each operable to pre-fetch data from the processor memory and to store the data in the local cache for use by a corresponding peripheral device, Sharma discloses the use of prefetching in an I/O processor in column 4 lines 12-19. Sharma states that by prefetching data to be placed in an I/O processor cache in the manner disclosed reduces the latency of the system. Therefore it would have been obvious to one of ordinary skill in the art at the time of invention to prefetch data into a I/O cache to increase system performance.

In regards to claim 17, Barroso does not disclose pre-fetching data from the processor memory system; and

caching the data in an interface for use by a corresponding peripheral device, Sharma discloses the use of prefetching in an I/O processor in column 4 lines 12-19. Sharma states that by prefetching data to be placed in an I/O processor cache in the manner disclosed reduces the latency of the system. Therefore it would have been obvious to one of ordinary skill in the art at the time of invention to prefetch data into a I/O cache to increase system performance.

Response to Arguments

Applicant's arguments filed 29 November 2004 have been fully considered but they are not persuasive.

Applicant's amendment to claims 1, 9 and 22 is a broader rephrasing of dependent claims 21 and 25, these dependent claims stood as rejected in the previous office action, the rejection of claims 21 and 25 were not addressed in applicant's response other than to make a general claim that Bourne et al. does not disclose the teach applicant's amended claim. The examiner asserts that the limitation "wherein a copy of data is outdated upon expiration of a time period for the storage of the copy" is more narrow in scope than the limitation "the local caches of the I/O subsystem operable to participate in the coherence domain through timed access to data in the processor system." Since the more narrow limitation stood as rejected under 35 USC §103 in the previous office action, and the applicant did not provide how applicant's

claimed invention is distinct from the combination of Barroso and Bourne, the claims remain rejected under this combination.

Applicant states Barroso does not anticipate that claim 18 because Barroso fails to teach the limitation "a resource manager operable to invalidate outdated data from the local cache to maintain coherence with the processor memory." The examiner believes the applicant is reading limitations into the claim that do not exist. The term "outdated data" does not suggest the expiration of a time period; it only refers to data that is no longer useful. As such, data which is invalidated due to data becoming stale can be considered as outdated, therefore Barroso does anticipate applicant's claim 18 in its entirety.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul A Baker whose telephone number is (571)272-4203. The examiner can normally be reached on M-F 10am-6:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on (571)272-4210. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

PB

3/6/05

MANO PADMANABHAN
SUPERVISORY PATENT EXAMINER